

## Notice of References Cited

Application/Control No.

O9/972,100

Examiner

A. M. Thompson

Applicant(s)/Patent Under Reexamination RANKIN, ANDREW

Art Unit
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## U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	. Name	Classification
	Α	US-6,526,562	02-2003	Haddad et al.	716/18
	В	US-6,470,482	10-2002	Rostoker et al.	716/6
	С	US-			
	D	US-			
	E	US-		·	
	F	US-			
-	G	US-			_
	н	US-			
	1	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0				***	
	Р					
	Q					
	R					
	s					
	Т					

## **NON-PATENT DOCUMENTS**

*	* Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)					
		Piguet et al., Gate-Array and ASIC Standard Cell Libraries, Technology Leadership Data 200, HES Fribourg, pates 1-8, Octobe				
	U	2001.				
	٧	S. Zebardst et al., SP2V: Accelerating Post-Layout Spice Simulation Using Verilog Gate-Level Modeling. Canadian Conference on Electrical and Computer Engineering, Volume 1, pages 253-257, May 2001.				
	w	M. Naum et al., Automatic Functional Model Validation Between Spice and Verilog, 30th Industry Applications Conference, pages 1076-1083, October 1995.				
	x	•				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.